HANDS-ON

CONTINUOUS-TIME DELTA-SIGMA MODULATOR

June 23-25 and June 27, June 30, July 2 and 4, 2025

7-Days Online Course using Microsoft TEAMS

This course is intended to get the students' feet wet by designing a continuous-time delta-sigma modulator in their circuit simulator. The idea is to start from scratch and go step-by-step to design (at the macro model level) a continuous-time delta-sigma modulator.

Each attendee will be given a specification (bandwidth, SQNR, thermal noise) target and a step-by-step day-to-day target that needs to be achieved. The next day's tasks can be attempted only if the previous day's work is complete. A macro model design that meets target specifications is expected to be completed at the end of five days. Advanced students can go further if they achieve their target earlier than scheduled by replacing some circuit building blocks with transistor-level blocks designed in their process technology.

The prerequisites for the course are:

a. Highly recommended having undergone the MEAD delta-sigma class

b. Must have access to MATLAB, the delta-sigma toolbox (free download), and the control-systems toolbox. (Other possibilities exist, but are not supported).

c. Must have access to a CAD tool (Cadence/Spectre) is preferred, though one might choose to use their company's own internal simulation software. LTSPICE, though free, is not recommended as many simulator-related aspects cause bugs unless one is deeply familiar with LTSPICE. Often undocumented and frustrating, these bugs can add unnecessary delays and be confused with design-related problems.

d. Enthusiasm and perseverance :-). Trust me, you will need both in ample measure.

Student Name	Signal Bandwidth	In-band SNR	In-band SQNR	Loop filter topology	Number of quantizer levels	Quantizer delay	DAC pulse	Supply Voltage	Common-Mode voltage
X1	100kHz	90	>102	CIFF-B	3	0.5 clock cycle	NRZ	1.5	0.75
X2	1MHz	90	>102	CIFF-B	5	0.5 clock cycle	NRZ	1.8	0.9
X3	500kHz	90	>102	CIFB	4	0.5 clock cycle	NRZ	1.2	0.6
X4	5MHz	85	>97	CIFF-B	7	0.5 clock cycle	NRZ	1.5	0.75
X5	25kHz	98	>110	CIFF	2	0.5 clock cycle	NRZ	1.8	0.9
X6	200kHz	90	>102	CIFB	5	0.5 clock cycle	NRZ	1.8	0.9

The course will proceed as follows. In the kick-off class, the students are given their target specifications (like the ones above) - a different one for each student, and a day-wise plan will be shared with them. The plan will also have links to MEAD lecture material (that the students will have since they have attended the MEAD class earlier). Links to public-domain video lecture material will also be given if the student needs to brush up on concepts.

The student is given a whole day to perform the tasks of the day, **and create the necessary documentation.** A predefined documentation template will be given, so that the reports of all students look uniform. There will be a 3-hour interaction session where the instructor will help debug, give feedback and practical tips on how to go about the design. These sessions will also foster student interaction so that they may all learn together.